

LINEARIZED DIGITAL PHASE-LOCKED LOOP METHOD

This application claims the benefit of U.S. Provisional
Application No. 60/203,610, filed May 12, 2000 and is hereby
5 incorporated by reference in its entirety.

Cross Reference to Related Applications

The present application may relate to co-pending
application Serial No. _____, (Attorney Docket No. 0325.00386)
10 filed December 21, 2000, Serial No. _____, (Attorney Docket
No. 0325.00387) filed December 21, 2000, Serial No. _____,
(Attorney Docket No. 0325.00388) filed December 22, 2000, Serial
No. _____, (Attorney Docket No. 0325.00389) filed December 22,
2000, and Serial No. _____, (Attorney Docket No. 0325.00390)
15 filed December 22, 2000, which are each hereby incorporated by
reference in their entirety.

Field of the Invention

The present invention relates to a method and/or
20 architecture for implementing phase-locked loops (PLLs) generally

0325.00391
CD00087

and, more particularly, to a method and/or architecture for implementing linearized digital PLLs.

Background of the Invention

5 Conventional approaches for implementing PLLs include the bang-bang approach which comprises taking snapshots of the phase error with respect to edges of incoming data. The bang-bang approach corrects on every data edge based solely on the direction (polarity) of the offset. As a result, a bang-bang system is never truly "locked". In the best case, a bang-bang system is nearly locked and makes a correction at every data edge (i.e., clocks are either switched clockwise or counter clockwise depending on the polarity of the phase offset). The bang-bang approach has the disadvantage of introducing excessive jitter in the resulting recovered clock since the clock is being shrunk or expanded at every edge.

15 Referring to FIG. 1, a circuit 10 implementing a conventional bang-bang approach for constructing digital phase locked loops is shown. The circuit 10 involves the use of over
20 sampling methods to determine in which quadrant of the clock the data edge resides. The quadrant information is then applied to an

0325.00391
CD00087

adjustment mechanism which moves the clock the appropriate direction at each interval. No information associated with the magnitude of phase error is retained or utilized. Polarity of the error and presence of a data transition are the only information
5 used to adapt the phase of the clock to the incoming datastream.

Referring to FIG. 2, a flow diagram 30 illustrating the operation of the conventional bang-bang circuit 10 is shown. The circuit 10 checks for a data edge and determines the relative polarity between the data and clock. If the polarity of the data relative to the clock is positive, the clocks are switched counterclockwise. If the polarity of the data relative to the clock is negative, the clocks are switched clockwise.

Since the circuit 10 does not use magnitude information, a transfer function is exhibited at the phase detector which has the characteristics typical of a bang-bang approach. Such detectors have an inability to tolerate large input signal distortion, such as the distortion that may be found at the end of typical wired media.

Summary of the Invention

The present invention concerns a method for synchronizing a clock signal to a data signal, comprising the steps of (A) detecting an edge of the data signal, (B) determining whether a position of the edge is within a zone and (B) if the edge is not within the zone, adjusting the clock signal towards the position of the edge.

The objects, features and advantages of the present invention include providing a method and/or architecture for implementing a linearized digital PLL that may (i) reduce the sorts of distortion associated with media induced effects, (ii) reduce duty-cycle-distortion (DCD) and/or (iii) reduce data-dependant-jitter (DDJ), (DCD and DDJ may be lumped into the single category of systematic jitter).

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a conventional bang-bang system;

FIG. 2 is a flow diagram illustrating the operation of the conventional bang-bang circuit of FIG.1;

FIG. 3 is a block diagram of a preferred embodiment of the present invention;

5 FIG. 4 is a block diagram of the logic block of FIG. 3;

FIG. 5 is a timing diagram illustrating example waveforms of the circuit of FIG. 3; and

FIG. 6 is a flow diagram illustrating an example operation of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 3, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 generally comprises a logic block (or circuit) 102 and a control block (or circuit) 104. The circuit 104 may be implemented as a control circuit configured to adjust the frequency of an output clock.

The circuit 104 generally comprises a circuit 110, a circuit 112, a circuit 114 and a circuit 116. The circuit 104 may also comprise a number of memory elements 118a-118n and a number of buffers 120a-120n. The circuit 110 may be implemented as an edge

0325.00391
CD00087

detection circuit. The circuit 110 may present a signal (e.g., DATAPULSE) to the logic block 102. The signal DATAPULSE may be generated in response to a signal (e.g., DI_N) and a signal (e.g., DI_P). The signals DI_P and DI_N may be a complementary pair of
5 signals. In one example, the circuit 110 may be configured to generate a pulse signal in response to a transition of a data signal. The circuit 112 may be implemented as a counter circuit. The circuit 112 may present a signal (e.g., DATA_VALID). The signal DATA_VALID may be used to indicate a locked mode of the circuit 100. The circuit 114 may be implemented, in one example, as a phase lock loop (PLL). The PLL circuit 114 may present a number of clock signals (e.g., PLL_CLK_0-PLL_CLK_N) to the circuit 116. The signals PLL_CLK_0-PLL_CLK_N may include true and complement forms of the signals.

15 The circuit 116 may be implemented as a multiplexer circuit. The circuit 116 may present a number of signals (e.g., CLK(A:D)). In one example, the circuit 116 may be implemented as a multiple input multiplexer that may present an output signal based on a control signal (e.g., SEL) generated by the logic block
20 102. The circuit 116 may be configured to select a number of the

0325.00391
CD00087

signals PLL_CLK_0-PLL_CLK_N for presentation as the signals CLK(A:D) in response to the signal SEL.

The circuit 100 may implement a digital phase-detector (e.g., the logic block 102) that may be used as an integral part of a digital phase-locked loop for data and clock recovery circuits. Specifically, the digital phase-detector 102 may be used for linearization of the phase-detection and loop mechanisms to overcome the disadvantages associated with conventional systems (discussed in the background section of the present application).

Referring to FIG. 4, a more detailed diagram of the logic circuit 102 is shown. The logic circuit 102 generally comprises three major blocks, a phase-detector 122, a filter 124, and a phase-switcher 126. A preferred embodiment of the present invention, in its basic form, presumes a multi-phase reference clock controlled by the phase-switcher 126. The phase-detector 122 may be configured to detect the presence of a data-transition and compare the relative phase of the data-edge with that of the clock signals CLK(A:D). The relative phase is reduced to a numerical representation of the magnitude of the phase error between the data edge and the signals CLK(A:D), (e.g., between -N and +N, where N is the number of phases controlled by the phase-switcher 126).

0325.00391
CD00087

09740
10
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
2224
2225
2226
2227
2228
2229
2230
2231
2232
2233
2234
2235
2236
2237
2238
2239
2240
2241
224

0325.00391
CD00087

discrete-increment movement, of the clock phase edges into the system.

The phase detector 122 may comprise a register (e.g., REG1) and a circuit 130. The filter 124 may comprise a register (e.g., REG2). The phase switcher 126 may comprise a logic circuit 132, a register (e.g., REG3), a circuit 134 and a register (e.g., REG4). The circuit 130 may be implemented as a coder circuit. The circuit 132 may be implemented as an increment/decrement logic circuit. The circuit 134 may be implemented as a decoder circuit. In a preferred embodiment, the circuit 134 may be implemented as a 3 to 8 decoder.

The register REG1 generally receives the signals DATAPULSE and CLK(A:D) from the circuit 104. An output of the register REG1 may be presented to an input of the circuit 130. The circuit 130 may have an output that may present a signal to an input of the register REG2. The circuit 130 may generate the signal by encoding the polarity and magnitude of the phase differences between the data-edge represented by the signal DATAPULSE and the signals CLK(A:D). The register REG2 may have an output that may present a signal to an input of the circuit 132. The circuit 132 may have an output that may present a signal to an

0325.00391
CD00087

input of the register REG3. The register REG3 may present a signal to an input of the circuit 134. An output of the circuit 134 may be presented to an input of the register REG4. The registers REG2 and REG4 generally have a control input that generally receives the
5 signal CLK(A). The register REG3 generally has control input that may receive the signal CLK(B). The register REG4 generally presents the signal SEL in response to an output of the circuit 134.

The circuit 100 generally allows for the use of the detected phase error magnitude to emulate a linearized system having the characteristics at a macro level which approach a pure linear system. However, the circuit 100 may have resolution intervals allowing the simplicity of digital mechanisms to be implemented.

The advantage of the linearized system 100 over the pure digital PLL may be demonstrated by observation of the operation of the system 100 under high-levels of data stream distortion. Particularly, the operation of the circuit 100 may be observed under the sorts of distortion associated with media induced
15 effects, (e.g., systematic jitter, duty-cycle-distortion (DCD) and data-dependant-jitter (DDJ)).

Systematic jitter has the characteristics that the predominant effect is one of having few data transitions at the average location of the data edge. Rather, the data transitions may have a bi-modal distribution of the edge placements of the datastream at some $-M/+M$ location. When the data edges predominantly occur at locations $-M$ and $+M$ relative to the average location (or zero-phase) then any misalignment with the local clock cannot be determined by any single data edge placement.

The operation of the present invention may be easily demonstrated by considering a simple sequence. Presume an incoming datastream DI_N and DI_P is distorted such that the edges occur at $-J$ nS and $+K$ nS, where 0 nS is the ideal non-distorted location of the edges, or the 'average' location of the edges. Further presume that mechanisms associated with real systems during acquisition and normal operation are such that the magnitude of J and K are not necessarily equal. The conventional 'bang-bang' digital PLL would see $-J_1$, $+K_1$, $-J_2$, $+K_2$, $-J_3$, $+K_3$, etc. and generate a response, as a control to the internal phase-switcher, which would cause the clock to decrement in phase, then increment, decrement, increment, etc, no matter what the values of J and K .

The theoretical fail point for the conventional system is $\frac{1}{2}$ the clock period of distortion of the incoming datastream, then reduced by addition of general system non-idealities, matching, and the presence of random jitter components in the datastream. The
5 theoretical limits of operation of the circuit 100 are generally limited only by the numerical resolution N, associated with the detection resolution increments, and for cases of N=4, about $\frac{1}{4}$ clock-period, also as above reduced by system non-idealities, matching, and random jitter in the datastream. The ability to
10 tolerate an additional $\frac{1}{4}$ clock-period of data distortion can make the difference between a device that is marginal or does not function with a particular media, and one that exhibits infinitely low bit-error-rates.

For the USB 2.0 specification (published April 2000 and
15 hereby incorporated by reference in its entirety), a conventional bang-bang digital PLL will be marginal, if operable, to the system specifications for datastream distortion. Alternative implementations of the phase-detector may vary primarily in the exact construction of the numerical slicing/detection method or
20 conversion of phase-alignment to a numerical value or input to the accumulator. Variants of the filter block 124 are ordinarily

0325.00391
CD00087

limited to the magnitude of the accumulator threshold level detection for enabling a phase-adjustment of the phase-switcher block 126. Other filter clock variants may allow for the effective detection limit to adapt to acquisition conditions to allow for combination of fast acquisition and maximum tolerance when acquired. The implementation variants of the phase-switcher 126 and reference clock functions are predominantly associated with the number of raw clock phases available (e.g., $2N$) for selection-switching, and the incrementer/decrementer and associated clock-mux design and timing.

The circuit 100 implements the clocks sampled by data method described in co-pending provisional application (Serial No. 60/203,616), which is hereby incorporated by reference in its entirety.

A detailed description of an operation of the logic block 102 will now be described. An incoming serial data signal DI_N and DI_P may be sampled on the rising and falling edges to generate the signal $DATAPULSE$. The signal $DATAPULSE$ may be used to clock the current values of the clocks $CLK(A:D)$ into the register $REG1$. The value of the register $REG1$ may be encoded into, in one example, a 3-bit signal (via the coder 130). However, other bitwidths may be

0325.00391
CD00087

implemented to meet the design criteria of a particular application. The output of the encoder circuit 130 is a 3-bit signal, the output may comprise one bit of polarity information and two bits of magnitude information. The coded value generally
5 represents the offset of the sampled clocks to the ideal sample point in the serial data stream. The coded value is generally clocked into the register REG2 on the falling edge of the signal CLKA (e.g., A(fall)).

A decision is then made depending on the current operation mode of the system. When the system 100 is in the high bandwidth (or acquire) mode, if the magnitude of the offset value is zero then no further action is taken (e.g., the Inc/Dec logic 136 is not enabled). However, if the magnitude of the offset is non-zero then the polarity of the offset is passed directly to the Inc/Dec logic 136, (e.g., the Inc/Dec logic 136 is enabled). The
15 value of the register REG3 is then incremented or decremented as indicated by the polarity of the offset value on the next falling edge of the clock signal CLKA. The register REG3 and the Inc/Dec logic 136 may be implemented as a 3-bit counter with wrap around
20 and single adjustment limits. The value of the register REG3 may

0325.00391
CD00087

be decoded into a 1 of 8 value that is clocked into the register REG4 on the next falling edge of the signal CLKA.

When the register REG4 is updated the select values into the PLL clock select multiplexer(s) 116 are changed, thus changing the mapping between the input PLL clocks (PLL_CLK_0-PLL_CLK_N) and the internally sampled clocks CLK(A-D). For example, where the input PLL clocks are all 480MHz clocks with 1/8 bit of phase difference, the selection may result in a 1/8 bit time phase adjustment on the sample clock CLKA.

The counter 112 may assert the signal DATAVALID at a first predetermined count (e.g., seven bit times). The circuit 100 may present the output clock as the inversion of the current CLKA. The data is generally recovered by sampling the data stream with a falling edge of the signal CLKA (e.g., through two D flip-flops) and then again with a rising edge of the signal CLKA (e.g., through a third D flip-flop) to ensure that it is synchronized with the output recovered clock.

Referring to FIG. 6, a method (or process) 200 is shown. The method 200 generally comprises a decision state 202, a state 204, a decision state 206, a decision state 208, a state 210 and a state 212. The decision state 202 generally determines if a data

0325.00391
CD00087

edge is present. If a data edge is not present, the decision state 202 continues to check for such a condition. If a data edge is present, the state 204 determines a relative polarity and phase-offset magnitude for the data and clock. The decision state 206
5 determines if the magnitude is within a predetermined zone. When the magnitude is within the zone, the process returns to checking for a data edge (e.g., the state 202). When the magnitude is not within the zone, the decision state 208 generally determines whether the polarity of the offset is positive or negative. If the polarity is positive, the state 210 switches the clock counter clockwise and returns to the state 202. If the polarity is negative, the state 212 switches the clocks clockwise and returns to the state 202.

The function performed by the flow diagram of FIG. 6 may
45 be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present
20 disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.